<table>
<tr><td>1</td><td>1</td><td>Mark is for AO1 (knowledge)

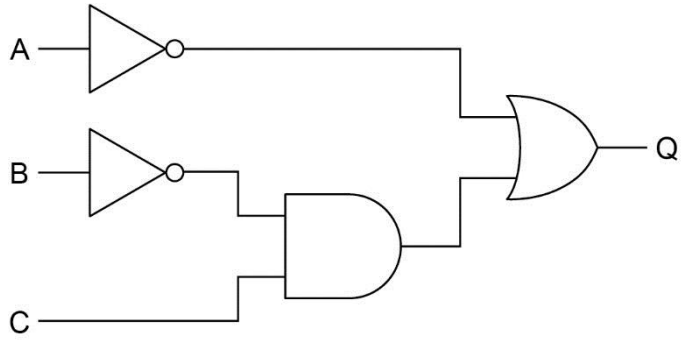
XOR // Exclusive OR // EOR // EXOR;</td><td>1</td></tr>
<tr><td>1</td><td>2</td><td>Mark is for AO1 (knowledge)

1 mark for correct column Q;

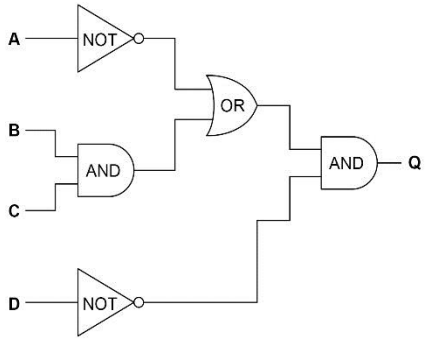
<table>
<tr><th>A</th><th>B</th><th>Q</th></tr>
<tr><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td></tr>
</table></td><td>1</td></tr>
<tr><td>1</td><td>3</td><td>Marks are for AO2 (apply)

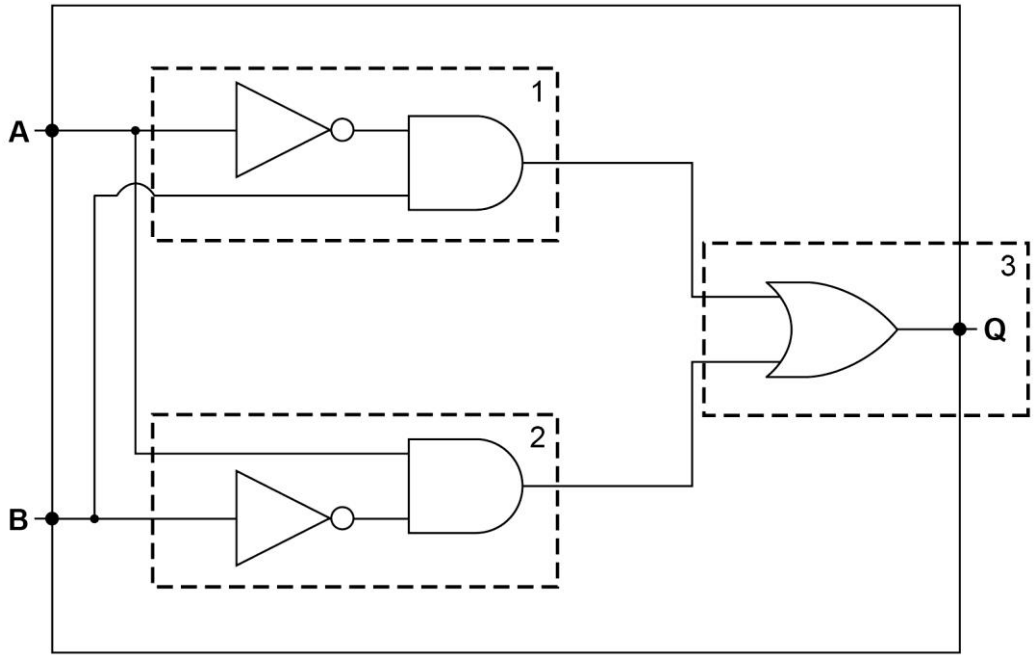
1 mark for having A and B connected to (different) NOT gates;

1 mark for an AND gate connected to C and to the output of a NOT gate;

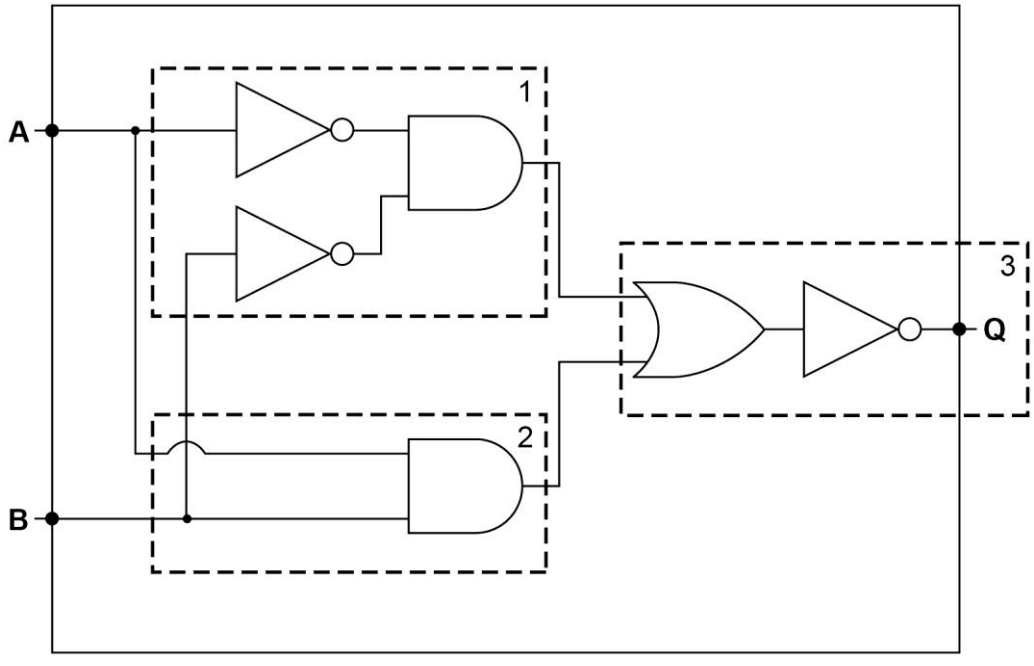
1 mark for an OR gate connected to NOT A and NOT B AND C and outputting to Q;</td><td>3</td></tr>
<tr><td></td><td></td><td> 

Max 2 if circuit not fully correct.</td><td></td></tr>
</table>

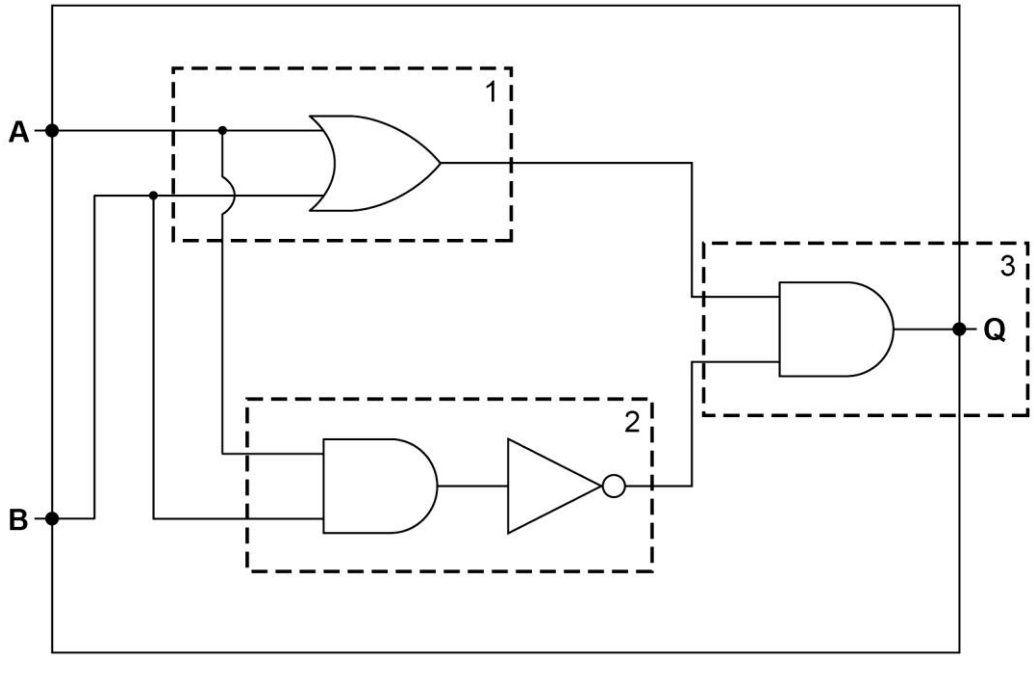
2	1	**Mark is for AO1 (knowledge)** NOR;	1
2	2	**Marks are for AO2 (apply)** **Mark as follows** **1 mark** for B and C into AND gate **1 mark** for the result of B and C (**I.** incorrect gate) as one input and a NOT gated A as a second input to an OR gate **1 mark** D connected to NOT gate and output of this to an AND gate, the results of A, B and C (**I.** previously incorrect gates) as the other input, with the output going into Q **MAX 2** if not fully correct  	3
2	3	**Mark is for AO1 (understanding)** OR; **A**. A+B // +	1

3	1	**Mark is for AO1 (knowledge)** **A** | **B** | **A NAND B** 0 | 0 | 1 0 | 1 | 1 1 | 0 | 1 1 | 1 | 0	1
3	2	**3 marks are for AO2 (apply)** **1 mark** for getting Part 1 **or** Part 2 correct on any of the three diagrams. **1 mark** for getting **corresponding** Part 1 **or** Part 2 correct on the same diagram. **1 mark** for getting **corresponding** Part 3 correct on the same diagram. **MAX 2** if not fully correct Mark response against diagram that will give the highest mark. Mark point 3 can only be awarded if at least one other mark point has been awarded. di Alternative Diagram 1  	3

Alternative Diagram 2

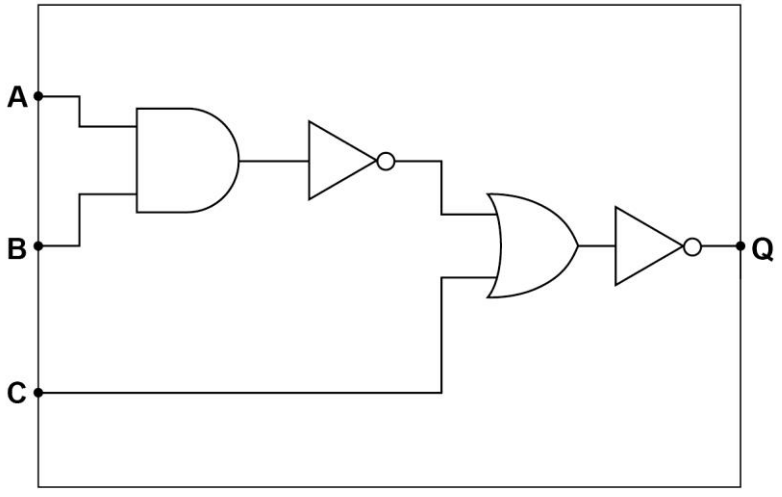
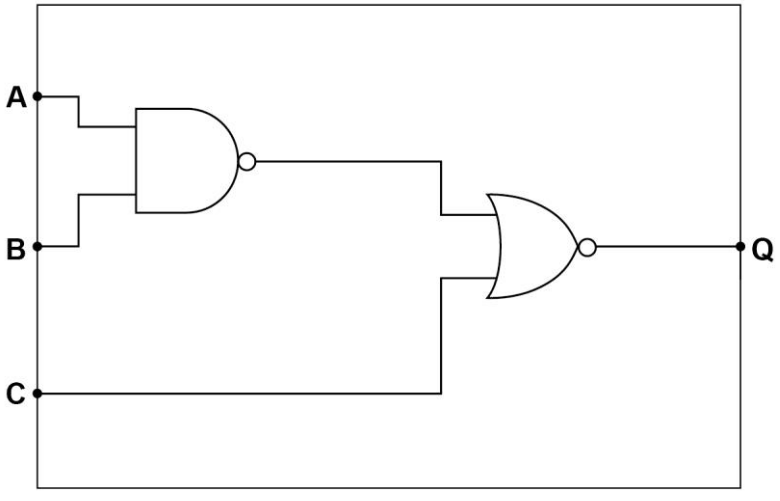


Alternative Diagram 3



Qu	Pt	Marking Guidance	Marks
4	1	**Mark is for AO1 (knowledge)** NOR;	1

Qu	Pt	Marking Guidance	Marks
4	2	**Mark is for AO1 (knowledge)** NAND; **R.** NOT AND	1

Qu	Pt	Marking Guidance	Marks
4	3	**Marks are for AO2 (application)** **1 mark** for each design point A and B are connected to the inputs of an AND gate and the output of the AND gate connected to the input of a NOT gate // A and B connected to the inputs of a NAND gate; The final two gates in the circuit are an OR gate followed by a NOT gate // The final gate in the circuit is a NOR gate; **A.** award 2 marks if the candidate has correctly simplified the Boolean expression and drawn a fully correct logic circuit. **MAX 1** if circuit does not correctly reflect the Boolean expression. **Possible answers:**   	2

<table>
<tr><th>Qu</th><th>Pt</th><th>Marking Guidance</th><th>Marks</th></tr>
<tr><td>4</td><td>4</td><td>
Marks are for AO2 (analyse)

1 mark for showing the correct truth table column for $\left(\mathrm{A}+\overline{\mathrm{B}}\right)\cdot\mathrm{B}$;

1 mark for showing the correct truth table column for $\left(\mathrm{A}+\overline{\mathrm{B}}\right)$;

<table>
<tr><th>$\mathbf{A}$</th><th>$\mathbf{B}$</th><th>$\overline{\mathbf{B}}$</th><th>$\left(\mathbf{A}+\overline{\mathbf{B}}\right)$</th><th>$\left(\mathbf{A}+\overline{\mathbf{B}}\right)\cdot\mathbf{B}$</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
</table>
1 mark for showing the correct answer as $\mathrm{A}\cdot\mathrm{B}$;
</td><td>3</td></tr>
</table>

Qu	Pt	Marking Guidance	Marks
5	1	**Marks are for AO2 (application)** **1 mark** for each highlighted column L, N and Y completed correctly. **A**. Follow through for Y if column N is completed incorrectly.	3

A	B	C	L	M	N	X	Y
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0
0	1	0	1	0	0	1	0
0	1	1	1	1	0	0	1
1	0	0	1	0	0	1	0
1	0	1	1	1	0	0	1
1	1	0	0	0	1	0	1
1	1	1	0	0	1	1	1

Qu	Pt	Marking Guidance	Marks
5	2	**Marks are for AO2 (application)** **2 marks:** $(A \oplus B) \cdot C + A \cdot B$ // $((A \cdot \bar{B}) + (\bar{A} \cdot B)) \cdot C + A \cdot B$ // $(\bar{A} \cdot B \cdot C) + (A \cdot (B + C))$ // **1 mark** for one of the following somewhere in the expression: • $(A \oplus B) \cdot C$ **I.** presence / absence of brackets around $A \oplus B$ • $((A \cdot \bar{B}) + (\bar{A} \cdot B)) \cdot C$ • $A \cdot B$ **Note:** If using a different algebraic notation refer to team leader.	2

Qu	Pt	Marking Guidance	Marks
06	1	**Mark is for AO1 (knowledge)** XOR // EXOR // EX-OR // Exclusive-OR // EOR;	1

<table>
<tr><th>Qu</th><th>Pt</th><th>Marking Guidance</th><th>Marks</th></tr>
<tr><td>06</td><td>2</td><td>
Marks are for AO2 (application)

1 mark for columns L and M correct

1 mark for column Z correct
A. follow through of incorrect values in columns L and M
<table>
<tr><th>A</th><th>B</th><th>C</th><th>L</th><th>M</th><th>Z</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table>
R. Entire column if more than one value shown in any cell of that column.
</td><td>2</td></tr>
</table>

<table>
<tr><th>Qu</th><th>Pt</th><th>Marking Guidance</th><th>Marks</th></tr>
<tr><td>06</td><td>3</td><td>
Marks are for AO2 (application)

Award full marks for showing correct expression:

$\mathrm{Q} = \overline{\overline{\mathrm{A}}.\,\mathrm{B}.\,(\mathrm{C}+\mathrm{D})}$

Max 2 marks for showing partially correct expression:

1 mark for showing $\overline{\mathrm{A}}.\,\mathrm{B}$

1 mark for showing of $\mathrm{C}+\mathrm{D}$

1 mark for using AND and NOT gates to combine and invert subexpressions

Full marks should be awarded for equivalent expressions.
</td><td>3</td></tr>
</table>

Qu	Pt	Marking Guidance	Marks
06	4	**Marks are for AO2 (application)** Marking guidance for examiners • Award marks for working out until an incorrect step has been made. • If, in any one step, a candidate is simplifying different parts of an expression simultaneously award all relevant marks for this multiple stage but don't award any further marks for working in any parts simplified incorrectly. Example, if the expression P.P.(P+Q) + P.P.1 was changed to P.(P+Q) + P.0, the candidate would get one mark for simplifying the first part to P.(P+Q) and could get further marks for correctly simplifying this part of the expression further but should not be awarded marks for simplifying the incorrectly changed part P.0 (ie to 0). Award up to **3 marks** for working. **1 mark per application** of a technique that produces a simplified expression. Of the 3 working marks **award at most 1 mark for correctly applying the Distributive Law** to expand or introduce brackets. **Note:** A simpler expression is one that is logically equivalent to the original expression but uses fewer logical operators. **1 mark** for final answer: $X \cdot Z + X \cdot Y + W \cdot Z$ or $X \cdot (Z + Y) + W \cdot Z$ **Example working 1:** $\overline{W} \cdot X \cdot Z + W \cdot Z + X \cdot Y \cdot \overline{Z} + \overline{W} \cdot X \cdot Y \cdot 1$ $\overline{W} \cdot X \cdot Z + W \cdot Z + X \cdot Y \cdot \overline{Z} + \overline{W} \cdot X \cdot Y$ Identity $A.1 = A$ $Z \cdot (\overline{W} \cdot X + W) + X \cdot Y \cdot \overline{Z} + \overline{W} \cdot X \cdot Y$ Distributive, put into brackets $Z \cdot (X + W) + X \cdot Y \cdot \overline{Z} + \overline{W} \cdot X \cdot Y$ $\overline{A}.B + A = B + A$ $X \cdot Z + W \cdot Z + X \cdot Y \cdot \overline{Z} + \overline{W} \cdot X \cdot Y$ Distributive, expand brackets $X \cdot \left(Z + Y \cdot \overline{Z}\right) + W \cdot Z + \overline{W} \cdot X \cdot Y$ Distributive, put into brackets $X \cdot (Z + Y) + W \cdot Z + \overline{W} \cdot X \cdot Y$ $\overline{A}.B + A = B + A$ $X \cdot Z + X \cdot Y + W \cdot Z + \overline{W} \cdot X \cdot Y$ Distributive, expand brackets $X \cdot Z + X \cdot Y \cdot \left(1 + \overline{W}\right) + W \cdot Z$ Distributive $X \cdot Z + X \cdot Y + W \cdot Z$ Identity $1 + A = A$ $X \cdot (Z + Y) + W \cdot Z$ (optional step)	4

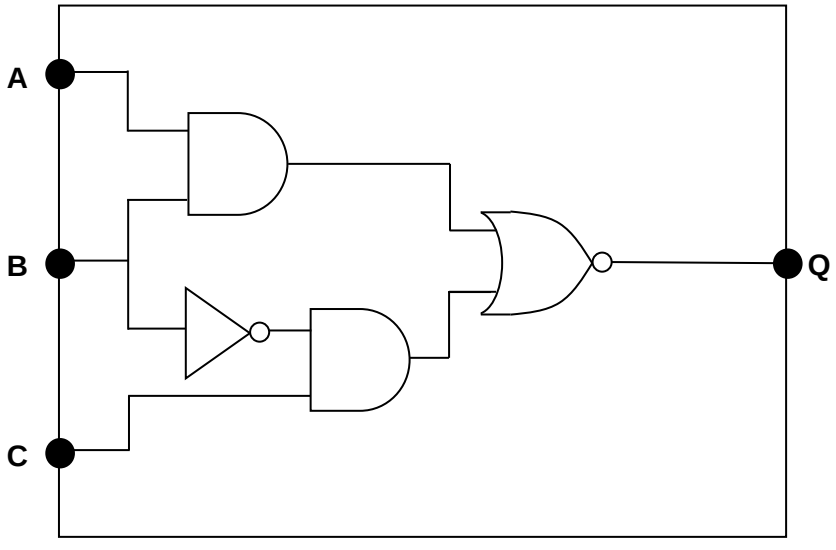
Example working 2 :

$\bar{W}.X.Z+W.Z+X.Y.\bar{Z}+\bar{W}.X.Y.1$	
$\bar{W}.X.Z+W.Z+X.Y.\bar{Z}+\bar{W}.X.Y$	Identity A.1 = A
$Z.(\bar{W}.X+W) + X.Y.\bar{Z}+\bar{W}.X.Y$	Distributive, put into brackets
$Z.(X+W) + X.Y.\bar{Z}+\bar{W}.X.Y$	Identity $\bar{A}.B + A = B + A$
$Z.X + Z.W + X.Y.\bar{Z}+\bar{W}.X.Y$	Distribution, expand brackets
$Z.W + Z.X + X.Y.\bar{Z}+\bar{W}.X.Y$	Re-arrange terms
$Z.W+ X(Z+\bar{Z}.Y) + \bar{W}.X.Y$	Distribution, put into brackets
$Z.W+ X(Y + Z) + \bar{W}.X.Y$	Identity $\bar{A}.B + A = B + A$
$Z.W + X.Y + X.Z + \bar{W}.X.Y$	Distribution, expand brackets
$X.Z + Z.W + X.Y + \bar{W}.X.Y$	Re-arrange terms
$X.Z + Z.W + X.Y$	Identity A + A.B = A

7	**1**	**Mark is AO1 (knowledge)** **OR Gate** **NAND Gate** **1 mark:** All values in both **Output** columns are correctly completed.	**1**

Inputs		Output
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

Inputs		Output
0	0	**1**
0	1	**1**
1	0	**1**
1	1	**0**

7	**2**	**All marks AO2 (apply)**  **1 mark:** Circuit inputs A and B connected as the inputs to an AND gate. **1 mark:** Circuit input B connected as the input to a NOT gate. **A.** NOT gate drawn as triangle without circle as BOD **1 mark:** Output of a NOT gate and C connected as the inputs to an AND gate. **A.** B and C going into AND gate if second mark point not awarded. **1 mark:** Outputs of two AND gates connected to a NOR gate as inputs which has its output connected to Q. **A.** correct use of OR and NOT gate instead of NOR gate. **Max 3** if circuit logic not fully correct **<u>Logically Equivalent Expressions</u>** If a response includes a statement of a logically equivalent expression for example $\overline{\mathrm{A}\,.\,\mathrm{B}}\,.\,\overline{\mathrm{C}\,.\,\overline{\mathrm{B}}}$ or $(\overline{\mathrm{A}}+\overline{\mathrm{B}}).(\overline{\mathrm{C}}+\mathrm{B})$ or $\overline{\overline{\overline{\mathrm{A}}+\overline{\mathrm{B}}}+\overline{\overline{\mathrm{C}}+\mathrm{B}}}$ then: • If the student appears to have drawn a circuit for the expression given to them on the question paper mark against mark points above. • If the student appears to have drawn a circuit for their logically equivalent expression refer the response to a team leader for marking. If a response includes a statement of an expression that is **not** logically equivalent then mark against mark points above.	**4**

8	**1**	**Mark is for AO1 (knowledge)** Table C; **R.** if more than one lozenge shaded	**1**

8	**2**	**4 marks for AO2 (apply)** Marks are awarded for the correct values in the unshaded cells only. **1 mark:** Correct values in columns A or C **1 mark:** Correct values in columns B or D **1 mark:** Correct values in column E **1 mark:** Correct values in column Q **Max 3** if any incorrect values in table	**4**

INPUTS				INTERMEDIATE POINTS					OUTPUT
X3	**X2**	**X1**	**X0**	**A**	**B**	**C**	**D**	**E**	**Q**
0	*0*	*0*	*0*	1	0	1	0	0	0
0	*0*	*0*	*1*	*1*	*0*	*1*	*0*	*0*	*0*
0	*0*	*1*	*0*	1	1	1	0	1	1
0	*0*	*1*	*1*	*1*	*1*	*0*	*0*	*1*	*1*
0	*1*	*0*	*0*	0	0	1	1	1	1
0	*1*	*0*	*1*	*0*	*0*	*1*	*1*	*1*	*1*
0	*1*	*1*	*0*	*0*	*0*	*1*	*1*	*1*	*1*
0	*1*	*1*	*1*	0	0	0	0	0	0
1	*0*	*0*	*0*	*1*	*0*	*1*	*0*	*0*	*1*
1	*0*	*0*	*1*	1	0	1	0	0	1

8	**3**	**Mark is for AO2 (analyse)** b; **A.** the middle bar	**1**

Qu	Pt	Marking guidance	Total marks
9	1	**Mark is AO2 (apply)** $Q1=\overline{X2}.\overline{X1}.X0$; **A.** a logically equivalent expression	**1**

Qu	Pt	Marking guidance	Total marks
9	2	**All marks AO2 (apply)** **1 mark:** 1 row completed correctly **OR** **2 marks:** 4 rows completed correctly **OR** **3 marks:** 8 rows completed correctly	**3**

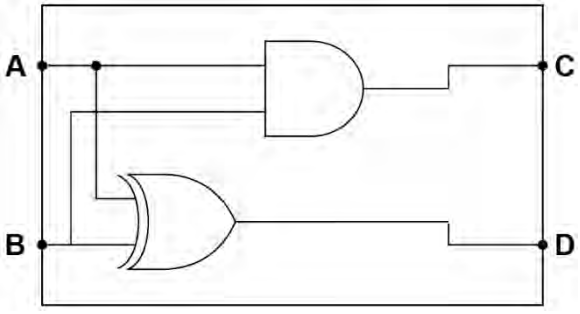
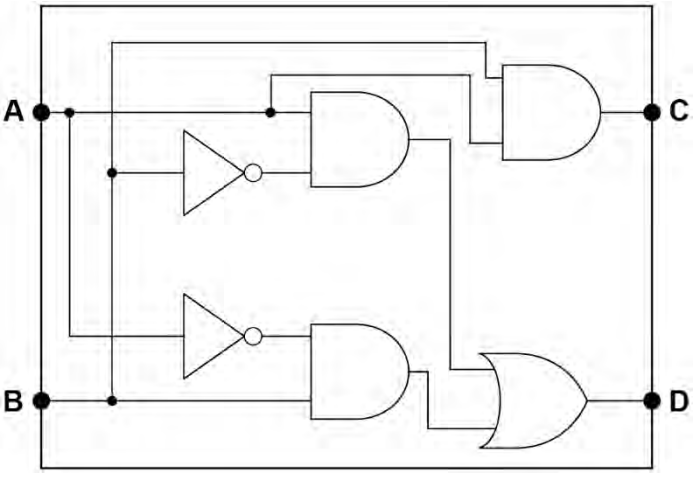
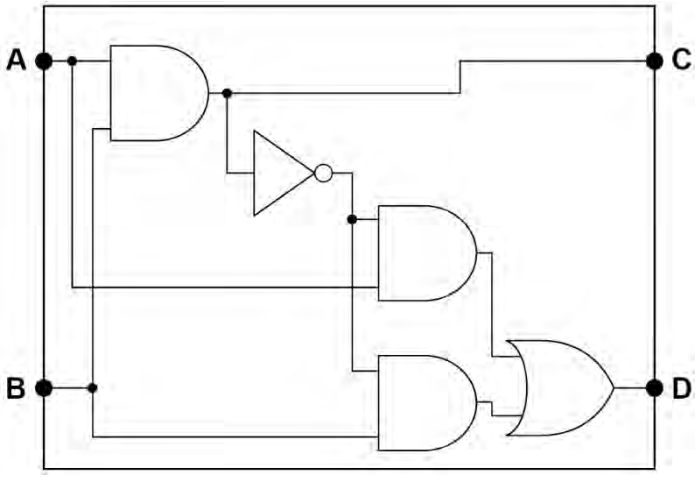
INPUTS			OUTPUTS							
X2	**X1**	**X0**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Qu	Pt	Marking guidance	Total marks
9	3	**All marks AO2 (analyse)** **2 marks:** Output **Qn** is 1 / on / activated when the binary pattern input is the value **n** **A. n** for **Qn** **A.** relationship between **n** and output **Qn** described by example eg if the value of the inputs is 0 then output 0 is on, if the value of the inputs is 1 output 1 is on, and so on. **A.** it is a (3-bit) binary decoder **OR** **1 mark:** One / a different output is 1 / on / activated for each different input pattern // it converts a binary input to a decimal output	**2**

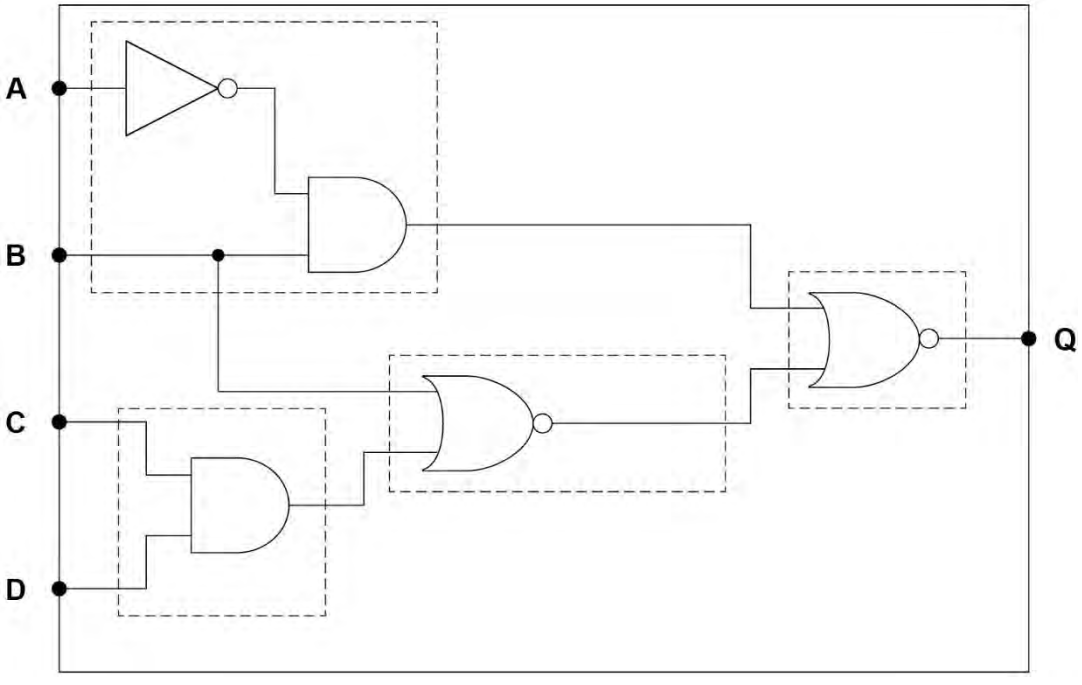
Qu	Pt	Marking guidance	Total marks
9	4	**Mark is AO2 (analyse)** **Q0;** **NE.** 0	**1**

Question			Marks
10	1	**Mark is AO2 (apply)** $\begin{array}{\|c\|c\|c\|c\|c\|c\|c\|}\hline \mathbf{A} & \mathbf{B} & \mathbf{A+B} & \overline{\mathbf{A}} & \overline{\mathbf{B}} & \overline{\mathbf{A}}\cdot\overline{\mathbf{B}} & \overline{\overline{\mathbf{A}}\cdot\overline{\mathbf{B}}} \\ \hline 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ \hline 0 & 1 & 1 & 1 & 0 & 0 & 1 \\ \hline 1 & 0 & 1 & 0 & 1 & 0 & 1 \\ \hline 1 & 1 & 1 & 0 & 0 & 0 & 1 \\ \hline \end{array}$ **1 mark:** Table correctly completed	**1**

Question			Marks
10	2	**Mark is AO1 (understanding)** De Morgan's (Law);	**1**

Qu	Pt	Marking guidance	Total marks
11	1	**All marks AO2 (apply)** **1 mark:** Output C is correct for all inputs **1 mark:** Output D is correct for all inputs **1 mark:** Circuit is fully correct and uses exactly two gates **Example Circuits** **3 mark solution:**  **2 mark solution:**  **2 mark solution: b**  	**3**

Qu	Pt	Marking guidance	Total marks
11	**2**	**Mark is AO2 (analysis)** It adds two bits (**A.** numbers) together // it is a half adder; **A**. it is an adder as BOD, it performs addition **R.** it is a full adder	**1**

Qu	Pt	Marking guidance	Total marks
12	1	**All marks AO2 (apply)**  **1 mark:** Circuit input A connected to a NOT gate. The output of the NOT gate and B connected as the inputs to an AND gate. **1 mark:** Circuit inputs C and D connected as the inputs to an AND gate. **A.** C and B connected to an OR gate, the output of which is connected to an AND gate with D as the other input (misunderstanding of precedence) **1 mark:** Circuit input B and output of an AND gate (not the same AND gate as first mark point is awarded for) connected as the inputs to a NOR gate. **1 mark:** NOR gate connected to circuit output Q. **A.** correct use of OR and NOT gates instead of NOR gate **Max 3** if circuit logic not fully correct.	**4**

Qu	Pt	Marking guidance	Total marks
12	2	**Mark is AO1 (understanding)** Output Q will change to (reflect current value of) D; **A.** if D=1, Q will be set to 1 and if D=0, Q will be set to 0 **A.** if Q and D are the same then Q will not change and if Q and D are different then Q will change **NE.** Q will update	**1**

Qu	Pt	Marking guidance	Total marks
12	3	**All marks AO2 (apply)** **Marking guidance for examiners** • Award marks for working out until an incorrect step has been made. • Ignore missing steps from the example solutions, as long as the jumps between steps are logically correct. • If, in any one step, a candidate is simplifying different parts of an expression simultaneously, award all relevant marks for this multiple stage but don't award any further marks for working in any parts simplified incorrectly. For example, if the expression P.P.(P+Q) + P.P.1 was changed to P.(P+Q)+P.0, the candidate would get one mark for simplifying the first part to P.(P+Q) and could get further marks for correctly simplifying this part of the expression further but should not be awarded marks for simplifying the incorrectly changed part P.0 (ie to 0). **1 mark** for final answer: $\mathrm{A} \oplus \mathrm{B}$ **A.** XOR instead of $\oplus$ **A.** $\overline{\mathrm{A}} \cdot \mathrm{B} + \mathrm{A} \cdot \overline{\mathrm{B}}$ **Max 3** for working. Award up to **three marks** for applying each one of the three techniques (**one mark** per application): • a successful application of De Morgan's Law (and any associated cancellation of NOTs) that produces a simpler expression • applying an identity other than cancelling NOTs that produces a simpler expression • successfully expanding brackets // factorising. **Max 2** for working if there is no successful application of De Morgan **Max 3** overall if any errors in working **Note:** A simpler expression is one that is logically equivalent to the original expression but uses fewer logical operators. **Example Solution (1)** $\overline{\mathrm{A}} \cdot (\mathrm{B} \cdot \mathrm{C} \cdot \mathrm{D} + \mathrm{B} \cdot \mathrm{C} \cdot \overline{\mathrm{D}} + \mathrm{B}) + \overline{\overline{\mathrm{A}} + \mathrm{B}}$ $\overline{\mathrm{A}} \cdot (\mathrm{B} \cdot \mathrm{C} \cdot (\mathrm{D} + \overline{\mathrm{D}}) + \mathrm{B}) + \overline{\overline{\mathrm{A}} + \mathrm{B}}$ Factorising $\overline{\mathrm{A}} \cdot (\mathrm{B} \cdot \mathrm{C} \cdot 1 + \mathrm{B}) + \overline{\overline{\mathrm{A}} + \mathrm{B}}$ By $X + \bar{X} = 1$ $\overline{\mathrm{A}} \cdot (\mathrm{B} \cdot \mathrm{C} + \mathrm{B}) + \overline{\overline{\mathrm{A}} + \mathrm{B}}$ By $X \cdot 1 = X$ $\overline{\mathrm{A}} \cdot \mathrm{B} + \overline{\overline{\mathrm{A}} + \mathrm{B}}$ By $X + X \cdot Y = X$ $\overline{\mathrm{A}} \cdot \mathrm{B} + \mathrm{A} \cdot \overline{\mathrm{B}}$ Application of De Morgan $\mathrm{A} \oplus \mathrm{B}$ Simplification to XOR	**4**

Example Solution (2)

$\overline{A} \cdot (B \cdot C \cdot D + B \cdot C \cdot \overline{D} + B) + \overline{\overline{A} + B}$	
$\overline{A} \cdot B \cdot C \cdot D + \overline{A} \cdot B \cdot C \cdot \overline{D} + \overline{A} \cdot B + \overline{\overline{A} + B}$	Expand brackets
$\overline{A} \cdot B \cdot C \cdot D + \overline{A} \cdot B \cdot C \cdot \overline{D} + \overline{A} \cdot B + A \cdot \overline{B}$	Application of De Morgan
$\overline{A} \cdot B \cdot C \cdot (D + \overline{D}) + \overline{A} \cdot B + A \cdot \overline{B}$	Factorising
$\overline{A} \cdot B \cdot C \cdot 1 + \overline{A} \cdot B + A \cdot \overline{B}$	By $X + \overline{X} = 1$
$\overline{A} \cdot B \cdot C + \overline{A} \cdot B + A \cdot \overline{B}$	By $X \cdot 1 = X$
$\overline{A} \cdot B + A \cdot \overline{B}$	By $X + X \cdot Y = X$
$A \oplus B$	Simplification to XOR

Example Solution (3)

$\overline{A} \cdot (B \cdot C \cdot D + B \cdot C \cdot \overline{D} + B) + \overline{\overline{A} + B}$	
$\overline{A} \cdot (B \cdot C \cdot D + B) + \overline{\overline{A} + B}$	By $X + X \cdot Y = X$ (where $X = B$ and $Y = C \cdot \overline{D}$)
$\overline{A} \cdot B + \overline{\overline{A} + B}$	By $X + X \cdot Y = X$ (where $X = B$ and $Y = C \cdot D$)
$\overline{A} \cdot B + A \cdot \overline{B}$	Application of De Morgan
$A \oplus B$	Simplification to XOR

Example Solution (4)

$\overline{A} \cdot (B \cdot C \cdot D + B \cdot C \cdot \overline{D} + B) + \overline{\overline{A} + B}$	
$\overline{A} \cdot B + \overline{\overline{A} + B}$	By $X + X \cdot Y = X$ – Award 2 marks as rule applied twice (where $X = B$ and $Y = C \cdot \overline{D}$ then $Y = C \cdot D$)
$\overline{A} \cdot B + A \cdot \overline{B}$	Application of De Morgan
$A \oplus B$	Simplification to XOR

Example Solution (5)

$\overline{A} \cdot (B \cdot C \cdot D + B \cdot C \cdot \overline{D} + B) + \overline{\overline{A} + B}$	
$\overline{A} \cdot (B \cdot (C \cdot D + C \cdot \overline{D} + 1)) + \overline{\overline{A} + B}$	Factorising
$\overline{A} \cdot (B \cdot 1) + \overline{\overline{A} + B}$	By $X + 1 = 1$
$\overline{A} \cdot B + \overline{\overline{A} + B}$	By $X \cdot 1 = X$
$\overline{A} \cdot B + A \cdot \overline{B}$	Application of De Morgan
$A \oplus B$	Simplification to XOR